<u>REMARKS/ARGUMENTS</u>

Claims 1, 3, 5-9, 11, 13-20, and 22-25 are pending in the application. The Applicants hereby request further examination and reconsideration of the application in view of these remarks/arguments.

In paragraph 5, the Examiner rejected claims 1, 3, 5, 7-9, 11, 14-20, and 22-25 under 35 U.S.C. § 103(a) as being unpatentable over Moeller (US2003/0170022, hereafter Moeller-022). In paragraph 6, the Examiner rejected claims 6 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Moeller-022 in view of Yonenaga. For the following reasons, the Applicant submits that all pending claims are allowable over the cited references.

Claim 1 is directed to a method of signal processing. The method has the steps of applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence.

In the rejection of claim 1, on page 3 of the office action, the Examiner admitted that Moeller-022 does not expressly disclose applying an "AND" function to the first and second bit estimate values to generate a bit of the bit sequence. However, on page 4, the Examiner stated that:

> Rather, Moeller discloses the application of an "OR" function (e.g., gate 260 in Fig. 2, gate 570 in Fig. 5) [and] the option of applying other alternative circuitry (paragraph [0020]). The usage of the "OR" function is to reduce the error probability for logical "1" values (paragraph [0027]). Logically speaking, an "AND" function is an "OR" function for "0" values. That is, a regular "OR" function outputs a "1" if any input is "1". Similar in operation, a regular "AND" function outputs a "0" if any input is a "0". At the time the invention was made, it would have been obvious to one of ordinary skill in the art to notice that such similar operation is an obvious variation of the method of Moeller. One of ordinary skill in the art would have been motivated to employ an "AND" function for the similar reason of employing an "OR" function, i.e., to reduce the probability of a particular bit estimate value, e.g., "0" values.

First, the Applicants submit that, as correctly noticed by the Examiner in the above-cited passage, changing the application of an "OR" function to the application of an "AND" function requires a recognition of the fact that incorrect decoding of optical "zeros," rather than optical "ones," can be a major source of decoding errors. However, that **recognition is absent** in Moeller-022 because Moeller-022 deals with decoding of optical return-to-zero (RZ) signals having a relatively small duty cycle, e.g., about 33% (see, e.g., Moeller-022's Figs. 3-4 and paragraphs [0018]-[0019]). When an optical signal has a small duty cycle, transmission impediments, such as jitter, do not increase the error probability for optical "zeros" (see, e.g., the last sentence of Moeller-022's paragraph [0026]). Therefore, there is no problem of incorrect decoding of optical "zeros" in Moeller-022, and it could not have been recognized there. In contrast, the present application recognized that, for optical signals broadened by dispersion and/or having a relatively large duty cycle, e.g., about 100%, incorrect decoding of optical "zeros" can be a major source of decoding errors (see, e.g., Applicants' Figs. 3A and 4A-B and page 5, lines 1-5).

Second, the Applicants submit that Moeller-022 does not suggest applying logical functions other than the "OR" function, the Examiner's statement to the contrary notwithstanding. More specifically, the relevant portion of relied-upon by the Examiner paragraph [0020] in Moeller-022 reads as follows:

> Although the front-end pre-amplified receiver **200** of FIG. 2 is depicted as a relatively complex receiver, a less complex conventional front-end pre-amplified

receiver can also be **implemented** within various embodiments of the present invention. Additionally, although the logic circuitry **260** of FIG. 2 is depicted as an OR logic gate, other circuitry or devices that are able to determine a resulting logic state of at least one input signal can be **implemented** with the concepts of the present invention. [Emphasis added.]

It is clear from the context of paragraph [0020] that what is being discussed here is **different hardware implementations of the same functionality**, and **not a different functionality** as implied by the Examiner. Indeed, the first of the above-cited sentences talks about replacing relatively complex front-end pre-amplified receiver **200** by a less complex receiver capable of performing the same function as receiver **200**. Likewise, the second of the above-cited sentences talks about replacing an OR logic gate with a different circuit capable of performing the same logic function as the OR gate. The Applicants submit that reading a suggestion of a logic function change into the above-cited text is unwarranted and improper.

Finally, and perhaps most importantly, changing the "OR" functionality of logic circuitry **260** to a different logic functionality, e.g., the "AND" functionality, would increase, rather than decrease, the number of decoding errors in receivers disclosed in Moeller-022 (see, e.g., Moeller-022's Fig. 4). The Applicants submit that a modification that would actually worsen the performance would not occur to one of ordinary skill in the art.

To summarize, Moeller-022 does **not** recognize that incorrect decoding of optical zeros can be a major source of decoding errors and does **not** suggest an application of a logical function other than the "OR" function for the purpose of correcting decoding errors. The Applicants submit that, in the absence of such recognition or suggestion, it would not have been obvious to one of ordinary skill in the art to change an "OR" function in Moeller-022 to an "AND" function, the Examiner's assertion to the contrary notwithstanding.

For all these reasons, the Applicants submit that the Examiner improperly used the teachings of Moeller-022 to reject claim 1, that claim 1 is allowable over Moeller-022, and that the rejection of claim 1 under 35 U.S.C. § 103(a) over Moeller-022 should be withdrawn. For similar reasons, the Applicants submit that claims 11 and 20 are also allowable over Moeller-022. Since the rest of the claims depend variously from claims 1, 11, and 20, it is further submitted that those claims are also allowable over Moeller-022. The Applicants submit therefore that the rejections of claims under § 103 have been overcome.

In view of the above remarks/arguments, the Applicants believe that the pending claims are in condition for allowance. Therefore, the Applicants believe that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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